

Lab 2

February 9, 2004

Transistors I: Gate-Source Dependence

In this lab we will be investigating the subthreshold behavior of isolated p - and n -channel MOSFET's. Specifically, we will measure the currents through the transistors as a function of their gate and source voltages; determine how effective these three terminals are at changing the current; and compare and contrast the characteristics of native and well devices.

Remember, you are studying the *subthreshold* behaviour, so make sure you choose your voltages and voltage ranges correctly!

2.1 Prelab

The questions will make much more sense if you read through the entire lab handout first. You are required to complete this prelab and have it checked before you can begin taking data.

For the following questions assume an n -well process—unless stated otherwise.

1. Draw four-terminal symbols for native and well transistors and label all the terminals; use **d** for drain, **s** for source, **g** for gate, **b** for bulk, and **w** for well. Indicate the direction of current flow that is consistent with your choice of drain and source.
2. Write expressions for the current I_{ds} in the channel for both types of transistors. Indicate how you would measure the voltages that appear in these expressions by adding voltmeters to the symbols you drew. (Hint: Think about what the appropriate reference voltage is.)
3. Obtain expressions for the saturation current of these transistors, that is the value of the current when V_d is more than $4kT/q$ away from V_s . For the remaining questions you may assume that the transistor is in saturation.
4. Briefly describe the difference between biasing a native and a well transistor. You should state explicitly what the signs of the terminal voltages should be, relative to the appropriate reference, and which rail of the power supply provides the reference.
5. For both a native and well transistor, derive an expression for gate voltage as a function of source voltage if the channel current is constant. In each case, what is dV_s/dV_g ?
6. By fabricating a well device in its own well, we can use the well as a second gate. This gate is called the back gate. Derive an expression for the current that shows explicitly the role of the back gate by using the source as the reference instead of the well. That is, replace V_g by $V_{gs} - V_{ws}$ and V_s by $-V_{ws}$ in the saturation current equation. What is the relationship between V_{gs} and $-V_{ws}$ if the current is constant? What is dV_{gs}/dV_{ws} ?

7. Draw the arrangements you will use in experiments 1, 2 and 3 of the lab for both native and well devices. Include the voltages you will be using to bias the fixed terminals of the device and the voltage range you plan on using to generate the required curve. Be explicit in showing the Keithley 6517 electrometer and the Keithley 2400 SourceMeter, and also which terminal of the instrument goes where¹. To make the in-lab work easier, it is a good idea to also include the pin numbers. Be sure to draw the setups for testing both the native and well transistors².

2.2 Equipment

You will be using the same equipment as in the previous lab (Keithley 2400, 6517 and 617), so refer to information handed out last week on those devices. In addition you will be using HP E3631A Triple Output DC Power Supply to power up the potbox (and chip).

2.2.1 Additional Information on Keithley 6517

The voltage source for the Keithley 6517 has a default current limit of 10mA. If the current limit is reached, the VOLTAGE SOURCE OPERATE light flashes. While in current limit, the programmed voltage is not being sourced. The current limit cannot be adjusted.

2.2.2 HP DC Power Supply

The DC power supply will be used to power the potbox. The device can provide up to three separate voltage supplies, range 0-6V, 0-25V, 0-(-25)V. When you power on the device, it will default to 6V range (text on the display should indicate +6V). If it is not, press the button marked +6V. Pressing Output On/Off button toggles output.

The display (when not indicating OUTPUT OFF) is divided into two sides. The left side indicates the output voltage level and the right side the output current level. To modify these levels, use the buttons found on the right side of the front panel. The Voltage/Current button switches between the voltage and current display (the blinking digit indicates which side and digit has control). The arrows are used to switch between digits; the knob is used to adjust the value.

The DC power supply has a current limit to provide protective measures. The current limit in these labs is very important, as you do not want to damage one of the chips due to incorrect wiring. To change the limits, press button marked *Display Limit*. *Lmt* will appear in small text along the bottom of the display. Adjust the limit levels using the same procedures as for adjusting voltage/current levels. When you current limit, text on the right side of the display will change from *CV* to *CC*.

¹It is not necessary to measure positive currents, you can easily swap sign once you have collected the data

²Some of the arrangements are given in this lab handout. Redraw them anyways to fully grasp the circuit connections

2.3 Automated Data Capture and Plotting

In this lab you will be using the PC workstation to capture all the data. To login, you will need an account set up on the machines. Ask the TA to setup an account. You will use this account for all future labs, so don't forget the password.

On the Desktop, there is a folder labeled for Lab02. Open the folder. There are two main icons that you will use. One is an application called *capture* and the other is a Mathematica Notebook called *Lab02.nb*.

Capture is the automated data capture program. This program is designed to interact with the Keithley 2400 and 6517 (or 617). Executing the program (by double clicking on the icon) brings up the control window. This window allows you to adjust the voltage range and the step size of the 2400 and also gives you the option of recording either current or voltage (depending on which part of the experiment) using the 6517 (617). In other words, the 2400 must be used as the control voltage and the 6517 must be used as the meter. Pressing the *Run* button will start the data capture. The data is automatically saved to a file (in the Lab02 folder) called *data.txt*. NOTE: if you want to save a set of data, rename the file, otherwise it will be overwritten the next time data samples are captured!

Double-clicking the Lab02.nb file will start Mathematica. This notebook is solely designed to provide a quick view of the data. Instructions on using Mathematica are found within the notebook.

You can use the PC to create the plots of your data and print them out. Otherwise you can ftp the data points to another account or save the file onto a floppy. **Remember: If you want save a data set, rename the file or save a copy elsewhere.** You can store all of your work on the machine. Ask the TA to setup a folder for you.

2.4 General facts about MOSFET chips

2.4.1 Static protection measures

All MOSFET chips are *extremely* prone to damage by static electricity. The current through the transistors is controlled by an insulated gate. Even a few tens of volts can blow out the gate. A short walk across the room can build up kilovolts of static potential. There are electrostatic discharge (ESD) protection structures on the chip inputs that are designed to leak off the static charge before it can damage the chip, but often this will not be enough.

There are two simple precautions that can definitely keep the chip safe.

1. **When the chip is not powered up in a socket, keep it stuck into a piece of black conductive foam.** This will short the susceptible inputs to both the power supply and ground pins.
2. **Always ground yourself to chassis ground before picking up or touching a chip.** This will discharge the static charge.

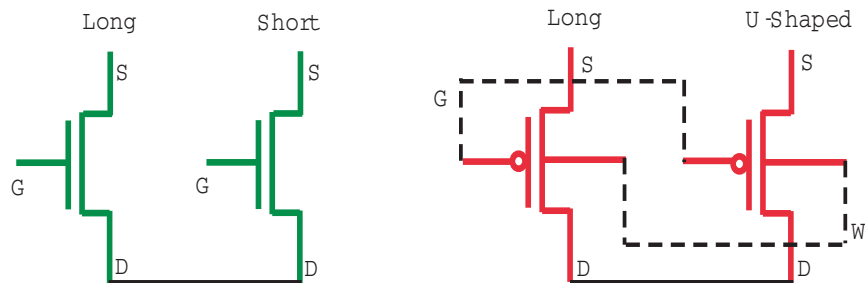


Figure 2.1:
Transistor types and pin labels on the class chip.

2.4.2 Powering up the chip

Before turning the power supplies on, hook up all the power and ground connections to the correct pins. You will need to supply V_{dd} and Gnd because even though we will be testing an isolated transistor the static protection structures on the gate need power, and the well needs to be biased correctly. These connections are already in place, so all you have to do is apply +2.5 volts across the V_{dd} and Gnd nodes.

Then, hook up whatever bias voltages you might need. Next, turn on the power supply, turn up the voltage to whatever you want (+2.5 volts for the n -well chips you will be testing), and then turn down the current limit until the voltage just begins to drop. Then turn up the current limit a little bit. This procedure will keep excessive current from flowing into your chip in the event you have screwed up the sign of the voltage or something else.

If the voltage from the power supply suddenly drops, it probably means you have something hooked up wrong and the power supply is current limiting. The chips we use should only draw a few milliamps.

2.4.3 The Classchip and Chip pinout labeling

The class chip has two n -well transistors and two p -well transistors. One is long (7/73 width/length in units of λ) and one is U-shaped (6/45+10+45 width/U-lengths). The pin labels for these transistors are shown in Figure 2.1. Remember, the source and the drain of any transistor is defined by their relative voltages. Therefore the labels may not actually represent the true source and drain of each transistor, as is apparent in Fig. 2.5

2.5 n -well process

Native transistors are transistors that lie directly in the substrate whereas well transistors are transistors that lie in wells. The classchip is an n -well chip. That means that the wells are n -type. Therefore native transistors have n -type sources and drains, and the well transistors have p -type sources and drains. The channels formed by the native transistors in the p -type substrate will be n -channels. A vertical section through the silicon with both native and well transistors is shown in Fig. 2.2.

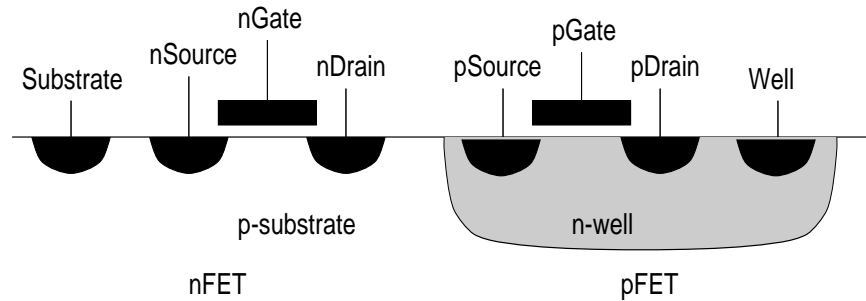


Figure 2.2:

A cross section through an n -well chip.

Since we are grounding the substrate and we are using an n -well chip, V_{dd} is at 2.5 volts. Question: what does this do to the junction between the wells (which are tied to V_{dd}) and the substrate (which is tied to Gnd)? When we slap together an n and a p region the diffusion of the mobile carriers sets up an electric field that drives the carriers back to their respective regions, holes to the p region, electrons to the n region. From this comes the saying, 'Carriers go home'.

In circuit schematics, the general convention we use is that when we draw a transistor *without* a bubble on the gate, it means we're indicating a native transistor, and conversely, a transistor *with* a bubble on the gate indicates a well transistor. This convention means that when we're using an n -well chip (like the classchip), the transistors without bubbles on the gate are n -channel transistors.

2.6 Experiments and Lab Reports

For the following experiments include in your lab reports graphs of all theoretical and experimental curves. Experimental data should be plotted in a point style so that individual data points are visible. Make sure you take enough data points! (For some mysterious reason, although it is just as easy to take 50 data points as to take 10 points with the computer controlled data acquisition programs, often students try to get away with taking as few points as possible.) The theoretical fit should be graphed on the same plot in a line style. Review the lab writeup guide before writing up your lab.

Remember that the purpose of this lab is to investigate *subthreshold* transistor characteristics. Therefore, all voltage sweeps should span the subthreshold regime.

2.6.1 The setup

You will be testing the long transistors (7/73 width/length in units of λ , where $\lambda = 0.12\mu\text{m}$) native and well transistors for all three experiments. Figure 2.3 shows the setup and pin labels for the native transistor for Experiment 1.

It is better to measure the current at the source as shown in Figure 2.3, although, in theory, there should be no difference between drain and source. Why is there a difference in practice? Remember that we will be measuring currents that are so small that they are comparable to leakage currents in the reverse-biased pn junctions.

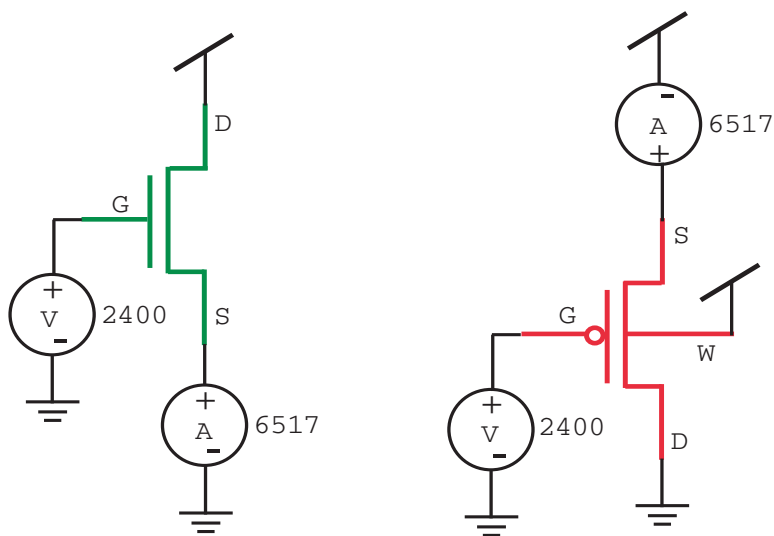


Figure 2.3:
Test setup for Experiment 1.

The 2400 will be used to sweep the voltage on the gate of the transistor while the 6517 (or 617, depending on your workstation), measures the current at the source. The positive side of the ammeter should *always* be nearest the chip. After manually checking whether your setup makes sense, use the **capture** program to take a rough curve of I_{ds} vs. V_g to see if everything is behaving as expected. A typical drain current will be about 1nA at a gate voltage of 0.25 volts. The current should increase about a decade for every 100 mV of gate voltage increase.

Obviously, the setup for the well transistor will be similar; the pin labels for the well device are: S (long), D, G, and W. During the experiment, you will apply the gate voltage from the positive terminal of the 2400. When comparing the well and native transistors in your analysis, it will be convenient to reference the gate voltage to V_{dd} .

It is very important to put the lid on the potbox when doing low-level measurements. The chips and instruments are very sensitive, and sometimes even breathing on the chip can make a large difference in the amount of leakage current. Be careful when you are taking data.

2.6.2 Experiment 1: Current as a function of gate voltage

For native and well transistors measure current as a function of gate voltage for fixed source, bulk (substrate or well), and drain voltages. Short the source to the bulk and bias the transistor into saturation.

Fit the theoretical expression you derived in the prelab to the data. You should include one plot for this experiment showing both native and well I_{ds} vs V_g curves with V_g referenced to the bulk. In other words, both curves should start at $V_g = 0$ on the left edge of the plot and increase to the right. That way, you can make a direct visual comparison of the two transistors in terms of their κ 's, their I_0 's, their threshold voltages, and the current at threshold. Based on the configuration of the 2400 and 6517 with the well device, you will

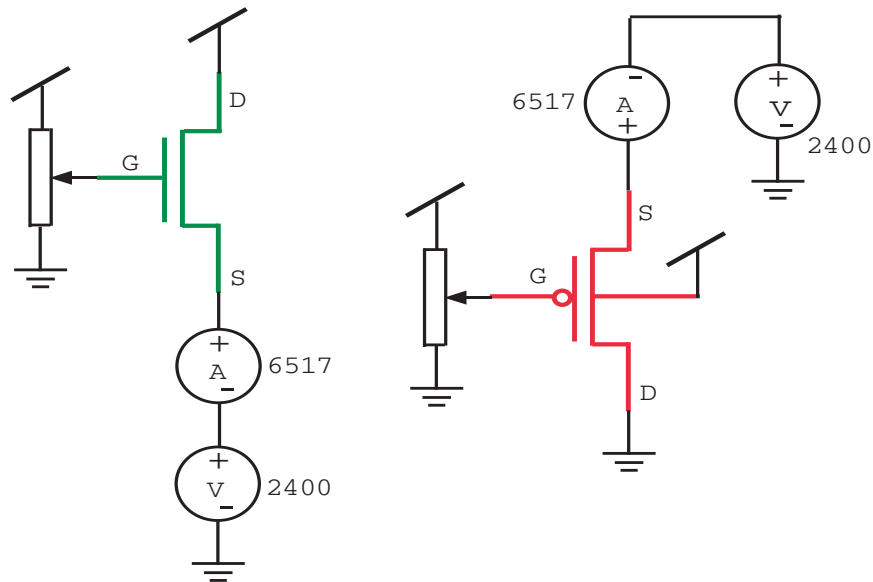


Figure 2.4:
Test setup for Experiment 2.

need to switch the sign of the well transistor currents, and subtract your applied V_g from V_{dd} , in order to make the proper comparison.

Compare and comment on the values of κ and I_0 you extracted from your theoretical fits for the two devices. Also, discuss any discrepancies between the values of I_0 extrapolated by the theoretical fits and the values you actually measured. Finally, extract the threshold voltage and the current at threshold, using the definition given in class. Compare and contrast the resulting values for the native and well devices. Does the difference in threshold currents correspond to the fact that electrons have 2.5 times the mobility of holes? Also compare the parameter values you obtained with those given my MOSIS test results for large devices (attached to the lab).

2.6.3 Experiment 2: Current as a function of source voltage

For this experiment, measure current as a function of source voltage for fixed voltages on the gate, drain, and bulk. Bias the transistor so that it is in saturation; make sure V_{ds} is at least 1.5V to minimize the effect of varying V_s , due to sweeping V_s , on the current.

Fit the expression from the prelab to the data. You should hand in a single plot with curves and fits for both devices. Compare the theoretical predictions with your experimental results. There will undoubtedly be discrepancies. Do you think the theory is flawed or the experiment is flawed? Why?

2.6.4 Experiment 3: The Back Gate Effect

The idea here is to characterize the relationship between the gate and source voltages for both a native and a well device when the channel current is held constant. This experiment

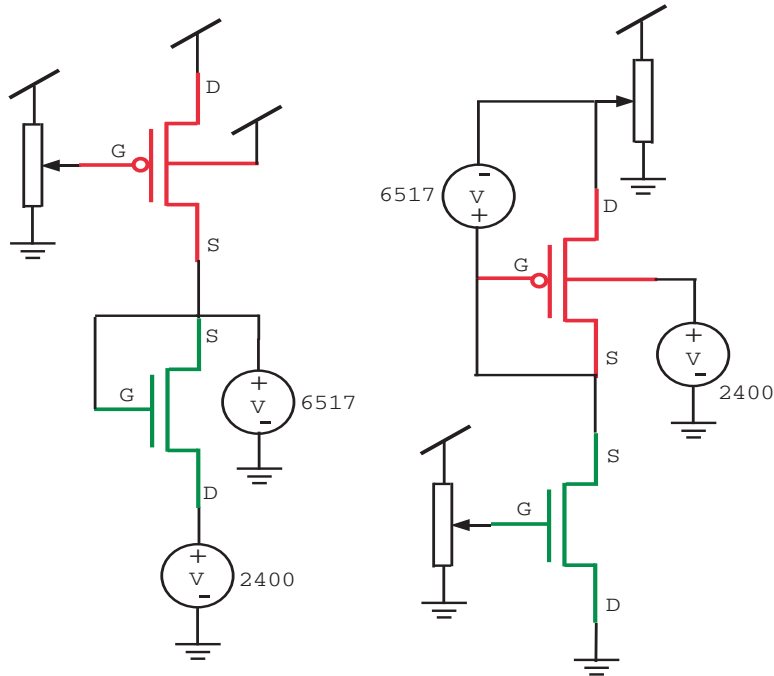


Figure 2.5:
Test setup for Experiment 3.

shows convincingly the relative effectiveness of each terminal and provides measurements of κ over the entire operating range. We shall use a transistor in saturation as a constant current sink or constant current source.

The setups for this experiment are shown in Figure 2.5:left. Use the well device as a current source; set the gate voltage to around 2.05V so that the transistor sources about 1 nA of current.

To test the native device, sweep its drain voltage from 0V to 1.5V and measure its gate voltage. Use a step size of 50mV. To obtain κ as a function of V_g , perform an approximate derivative on the data V_s vs V_g as follows:

$$\frac{dV_s}{dV_g} \approx \frac{V_s(i) - V_s(i-1)}{V_g(i) - V_g(i-1)} \quad (2.1)$$

where $V_s(i)$ & $V_g(i)$ are the i^{th} elements in your V_s & V_g vectors.

Hand in two plots: V_s and κ as a functions of V_g .

For the well device, (Fig. 2.5:right), use the native long transistor as a current sink, with its gate voltage around 0.25V for a 1nA bias current. Set the well-device (D) pin to 1.5V above Gnd using a potentiometer. Sweep the well from 0.0V to 1.5V *below* V_{dd} using the 2400 and measure the gate voltage. Remember that the gate and well voltages have the source as their reference (as in prelab). Do *NOT* take the well lower than the source voltage!

Take the approximate derivate, as above, of your V_{gs} vs. V_{ws} data and obtain κ vs V_{ws} using your result from prelab. Hand in plots of both sets of data.

Compare and contrast how much κ varies for these two devices. Identify the operating point of the transistors you measured in Experiment 1 on these curves and see whether the value for κ is the same.

Extra credit: Extract γ and ϕ_0 by fitting your measurements to the expression

$$\kappa = \left(1 + \frac{\gamma}{2\sqrt{\psi_s}}\right)^{-1} \quad (2.2)$$

where $\gamma = \frac{\sqrt{2qN_A\epsilon_{si}}}{C_{ox}}$ (as derived in class) and $\psi_s = V_s + \phi_0$, ϕ_0 being some constant.

How does your value for γ compare to that in the MOSIS sheet?

2.7 Postlab

For the following questions assume an n -well process with the transistor in saturation³.

Many differences in the properties of native and well transistors arise from the fact that the well is more heavily doped than the substrate. Well doping is large in order to overwhelm the carriers in the substrate and insure a predominance of the proper carrier type in the well. For a well device, the n -type material of the well is the bulk, while the active areas (source and drain) are p -type. The gate voltage must force all the electrons in the n -well away from the surface. The resulting depletion region provides a channel for holes through enemy territory (n -well) separating the p -type source and drain. Remember, an encounter with an electron will be fatal! If the bulk is heavily doped, the gate must work harder to repel electrons.

Another way of saying this is the capacitance of this depletion layer and the gate oxide capacitance form a capacitive divider that determines how much of the gate voltage appears at the surface channel. If the depletion layer is thin, the depletion capacitance will be large and hence the divider ratio will be unfavorable.

1. How does the depth of the depletion region depend on the doping and on the channel potential? Assume that the doping density is uniform.
2. Explain why κ varies with the source and well voltages.
3. Do the differences in bulk doping account for differences in κ between the native and well devices?
4. From your results in Experiments 1 and 3, state under what conditions the assumption that κ is constant is reasonable.

2.8 Next week

Transistors II: Drain-Source Dependence

³The answers to the postlab should be included with your lab writeup.